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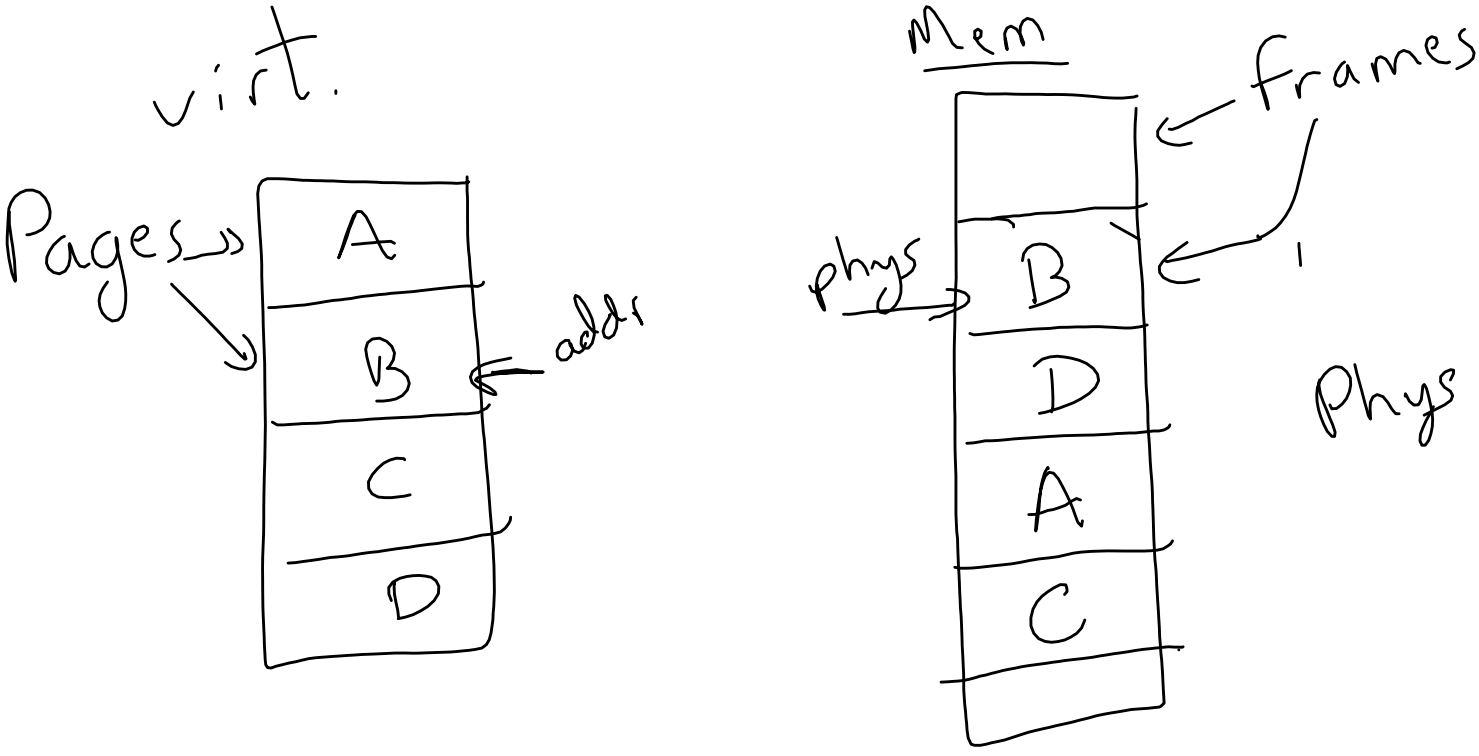
Paging

virtual addr → phys. addr



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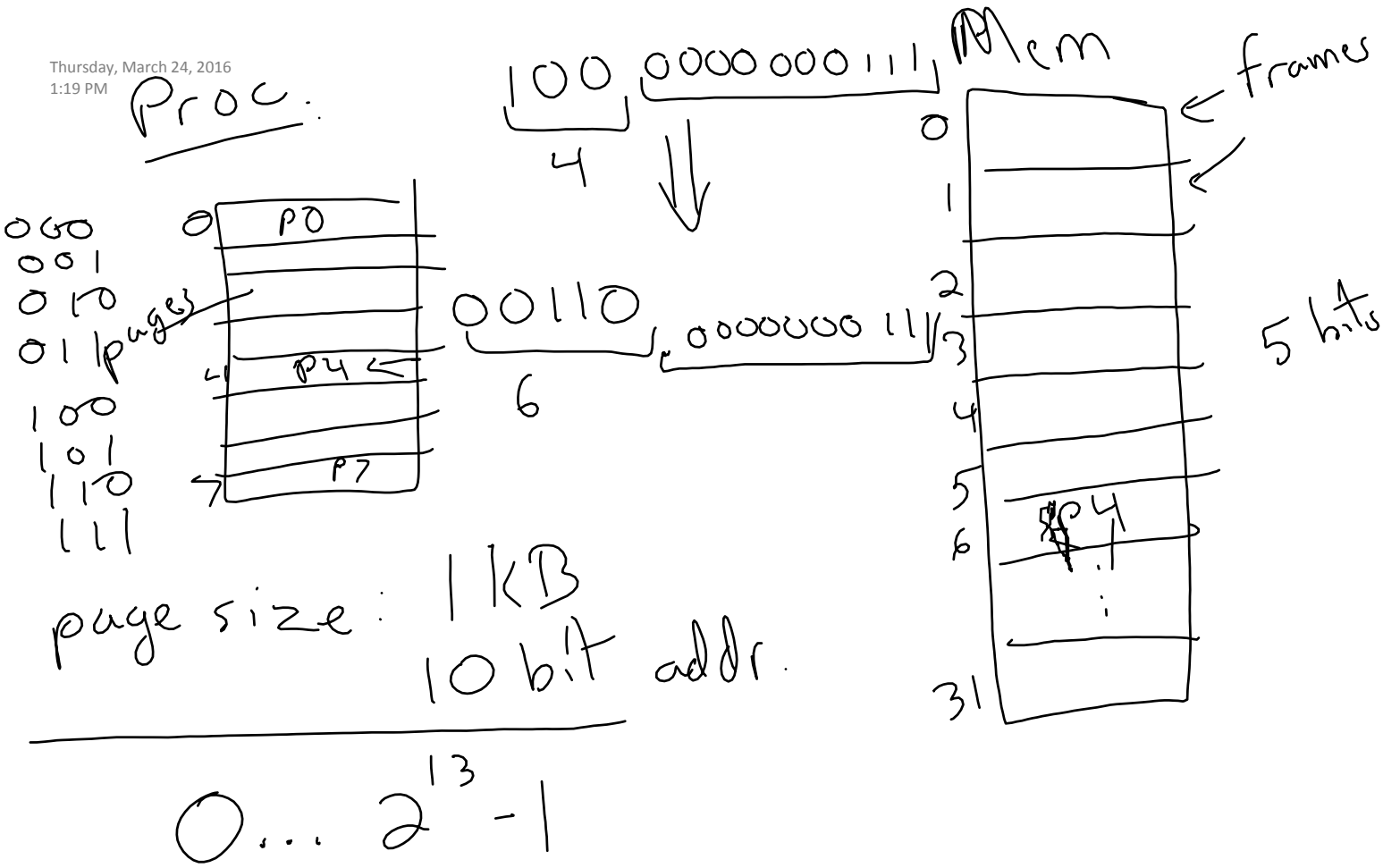

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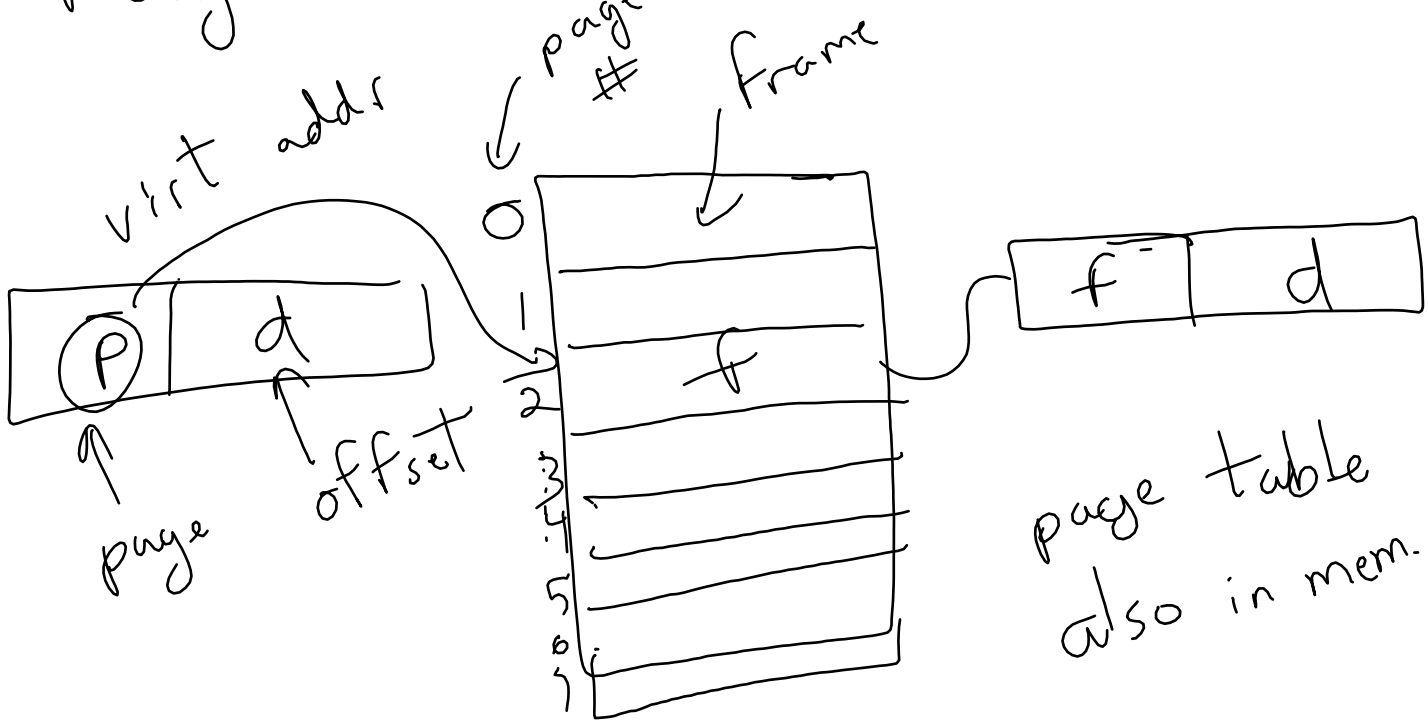
Page table ← process



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Free page list

- shared by processes
- bit map (one bit per frame)

Page table — multiple memory access

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TLB - hardware for paging
- translation look aside buffer
- cache of page table

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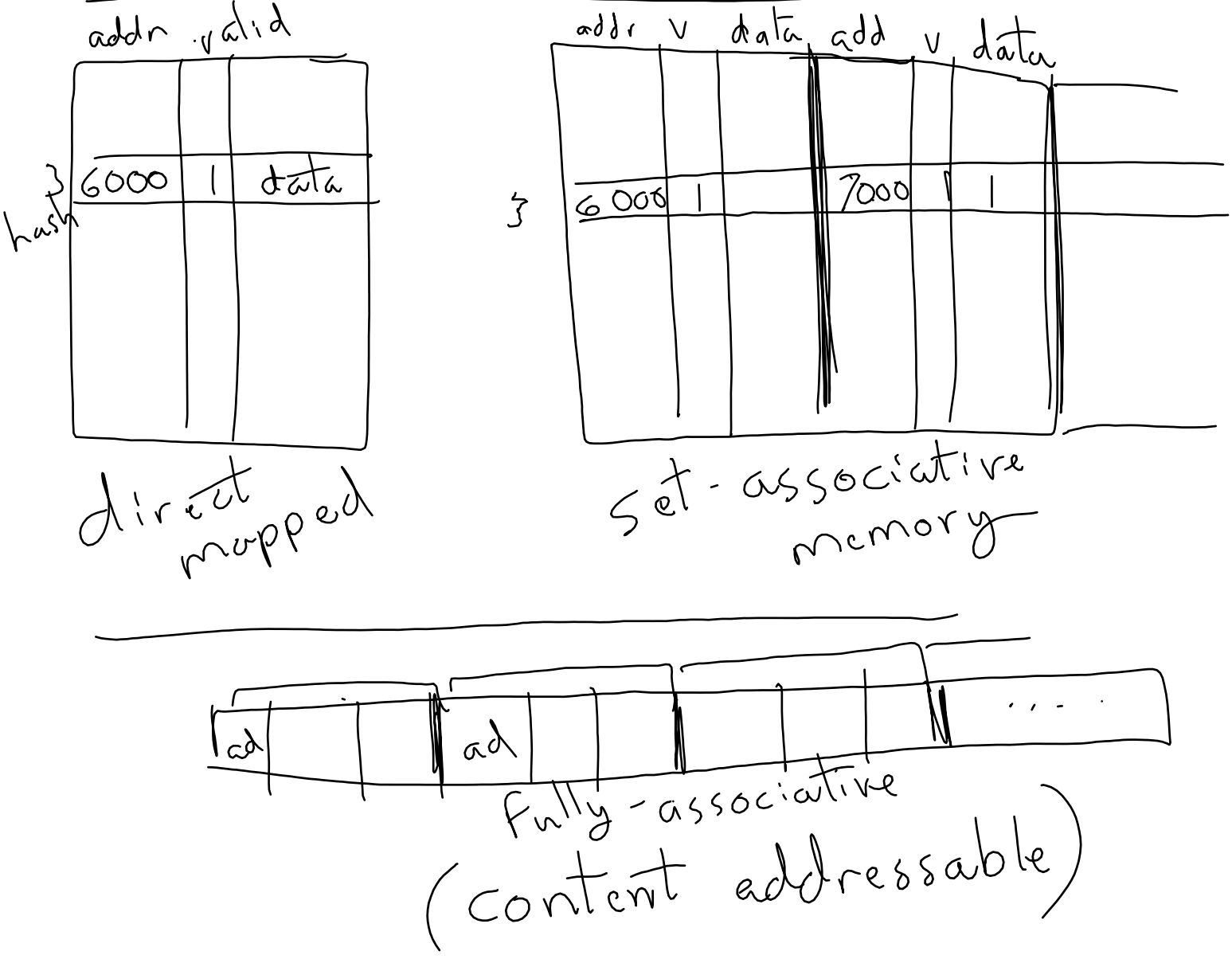
Cache implementation



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Cache operation

Is the address in cache?

yes – cache hit
bring data to CPU

no – cache miss
get data from memory
put it in cache
(remove other?)

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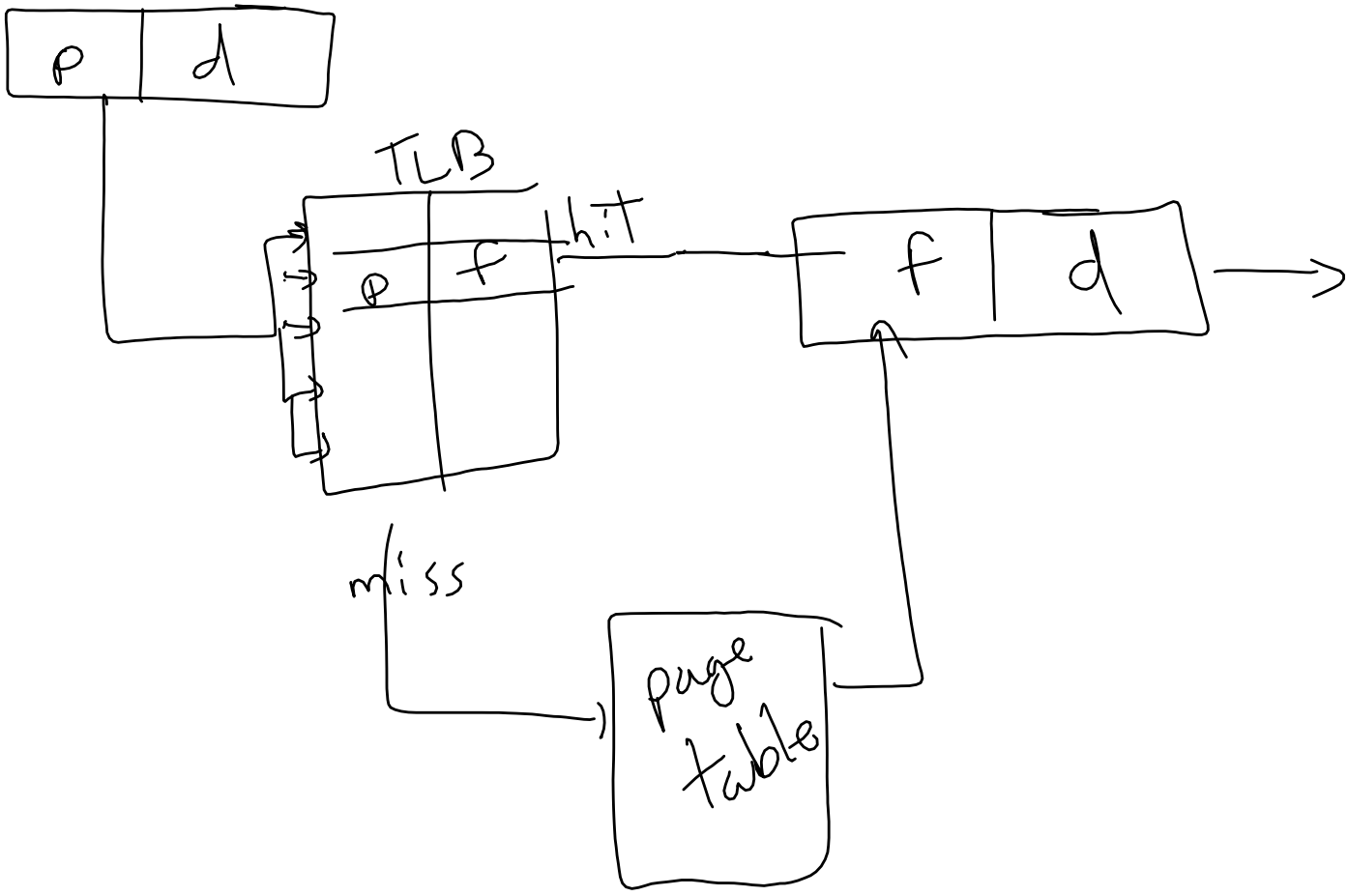
TLB



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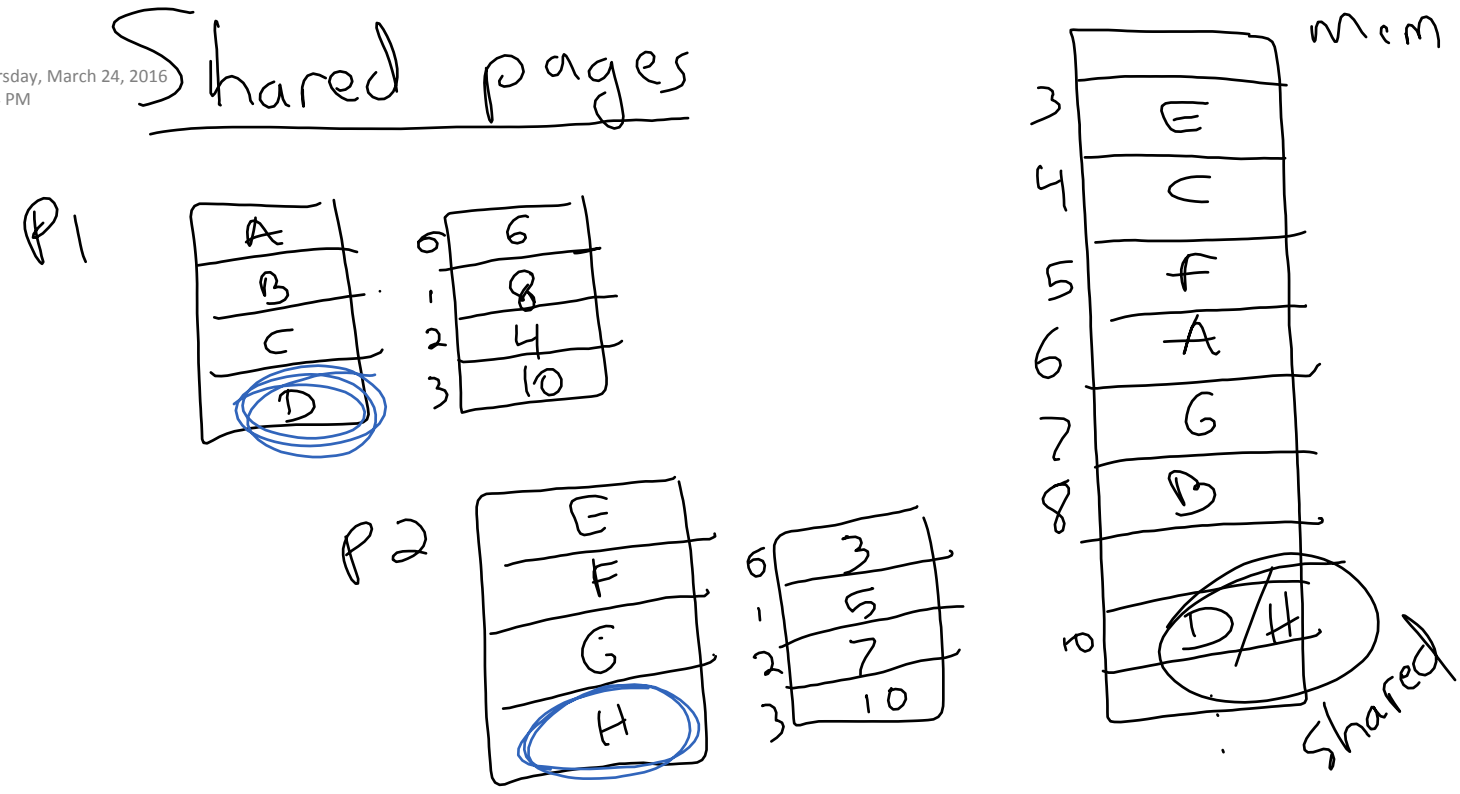
Shared pages



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32 bit logical addr

page/frame size 4 KB (2^{12}) ← offset

page number 20 bits

2^{20} page table entries

2^{22} = 4 MB page table

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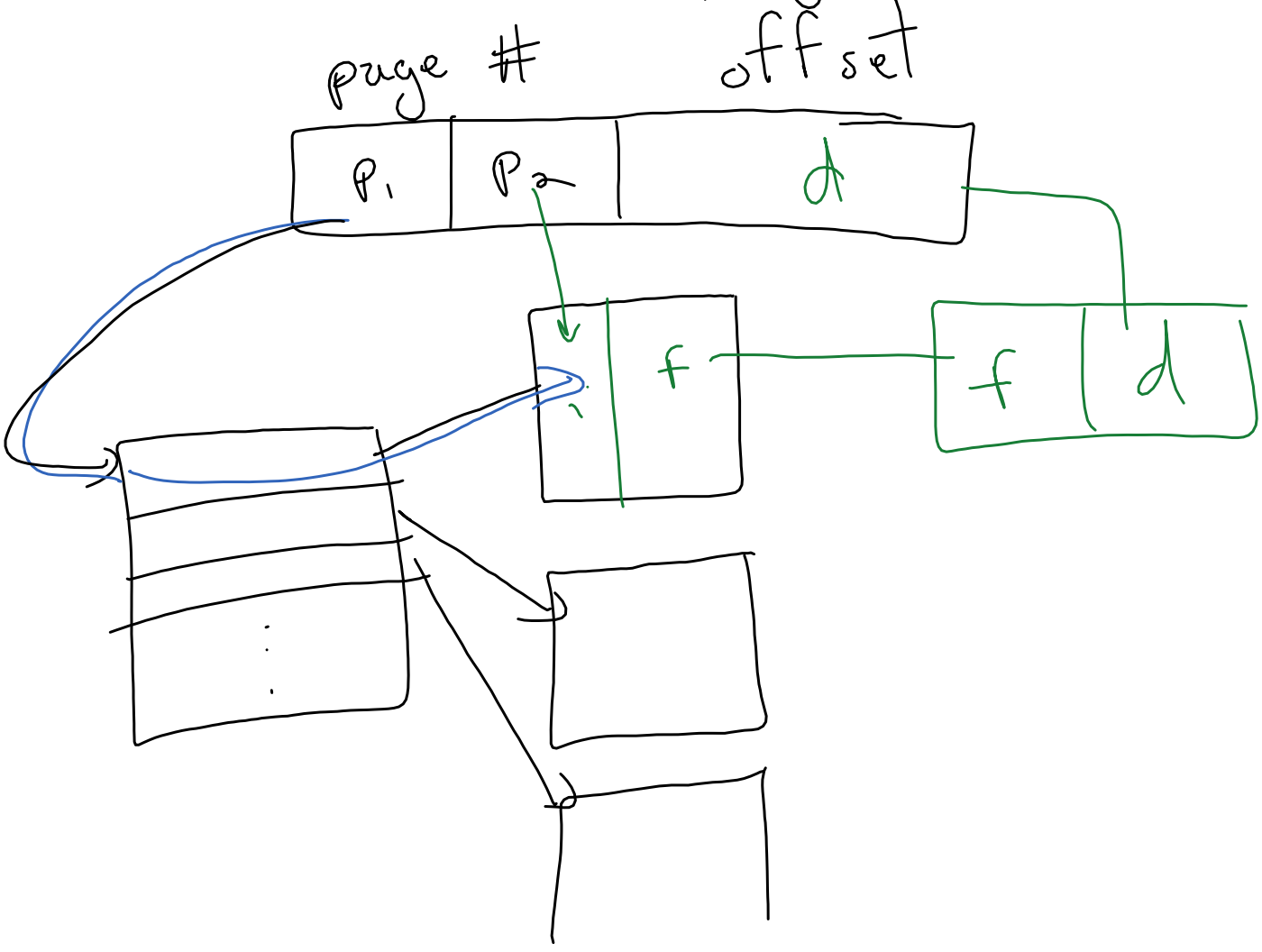
Hierarchical page tables



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Other types

- Hashed page table
- Inverted page table (frame table)