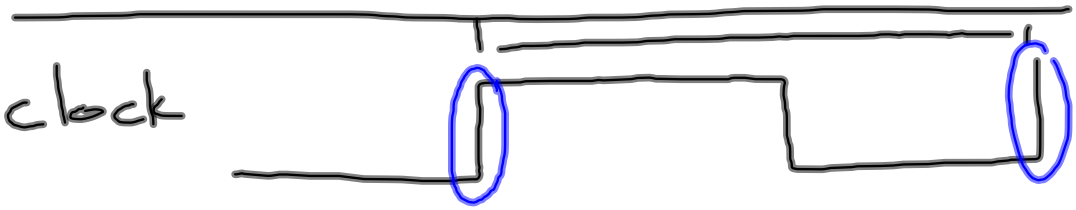
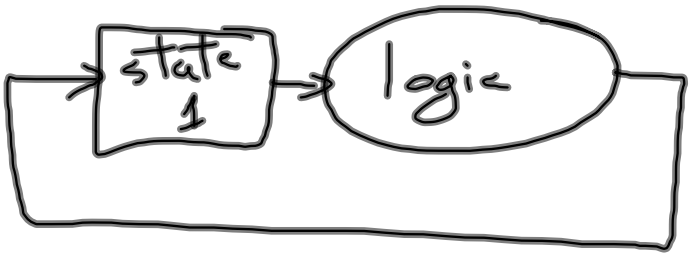
http://public.gettysburg.edu/~cpresser/cs221/ MIPS_Datapath.pdf

state devices - sequential
(memory, latches, registers)

logic devices - combinational
(circuits from truth tables)





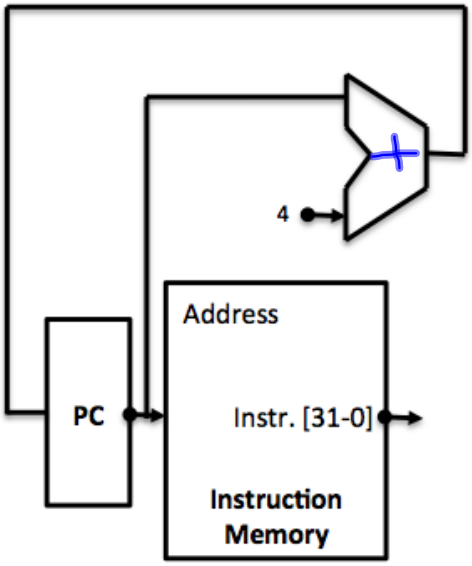


CPU

# Instruction Execution

1. fetch instr. from mem.
   - addr. in PC
2. Decode instr.
   - examine opcode/funct.
   - get registers ready for read/write
   - get operands
3. Execute
   - ALU does calculation
4. Memory access
5. Write result to reg (if any)

Instruction Fetch



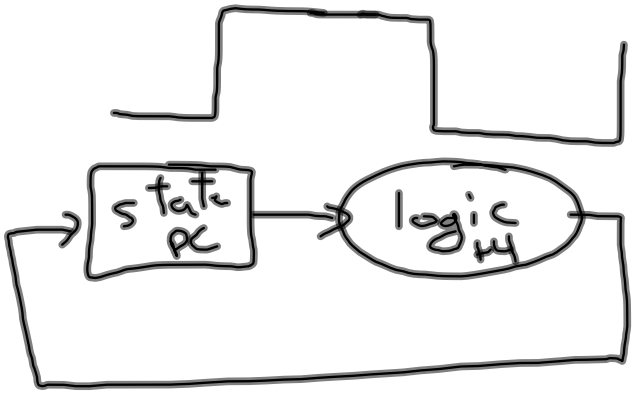
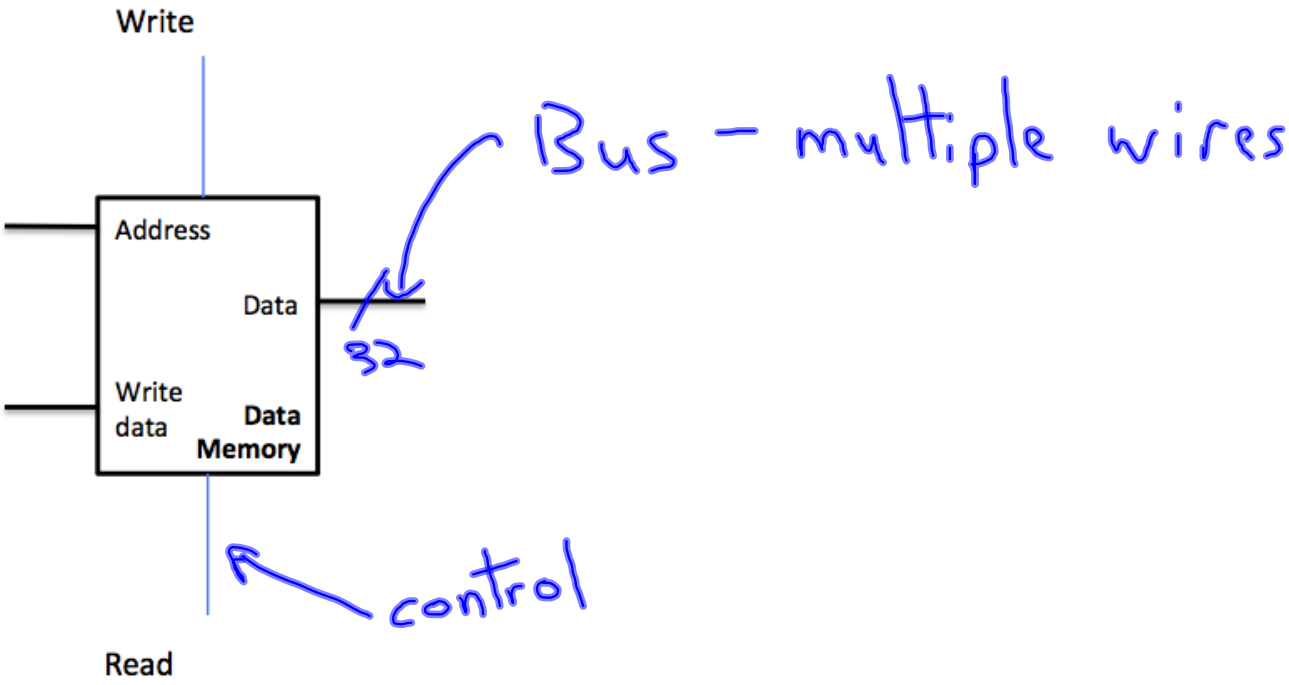
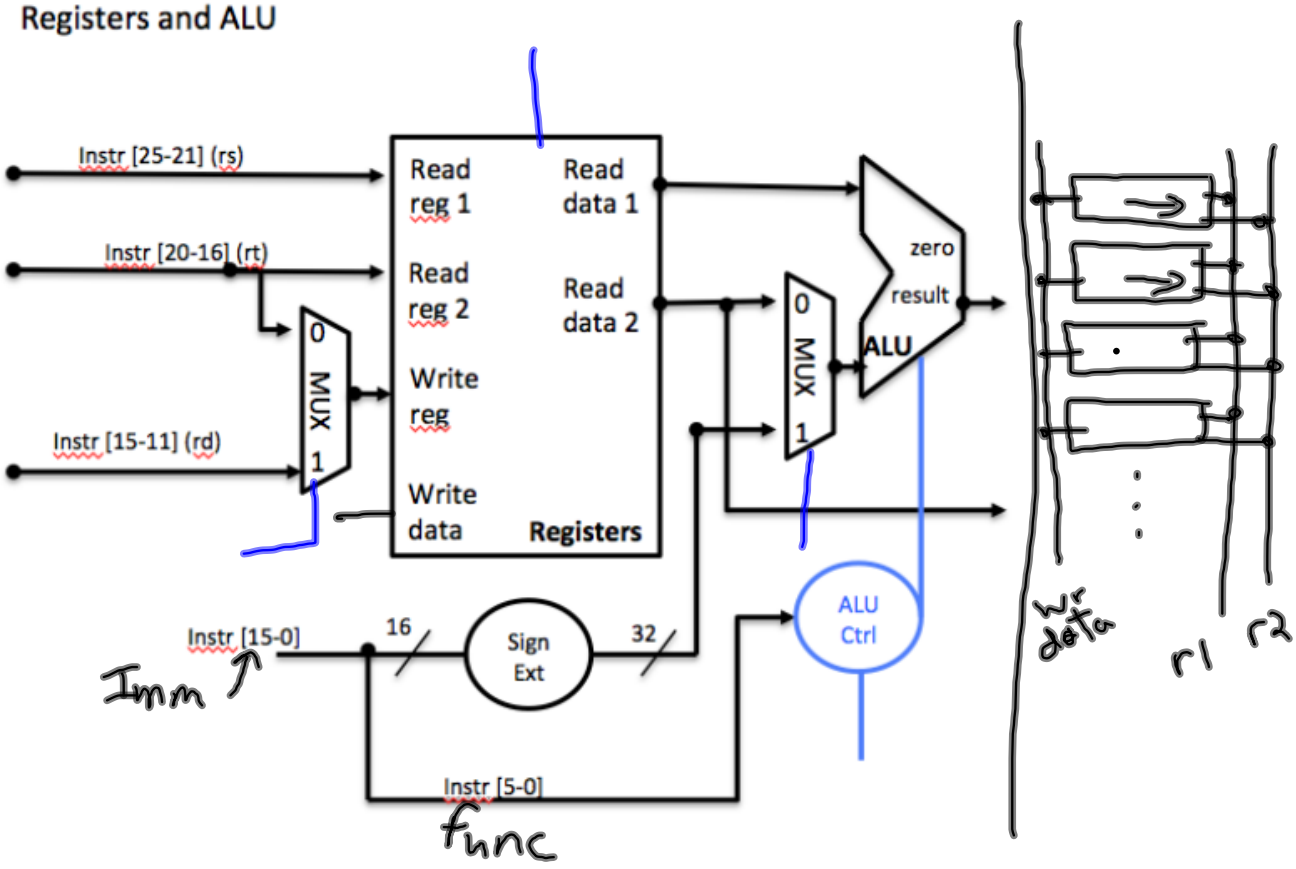




Fig 4.6 p 309

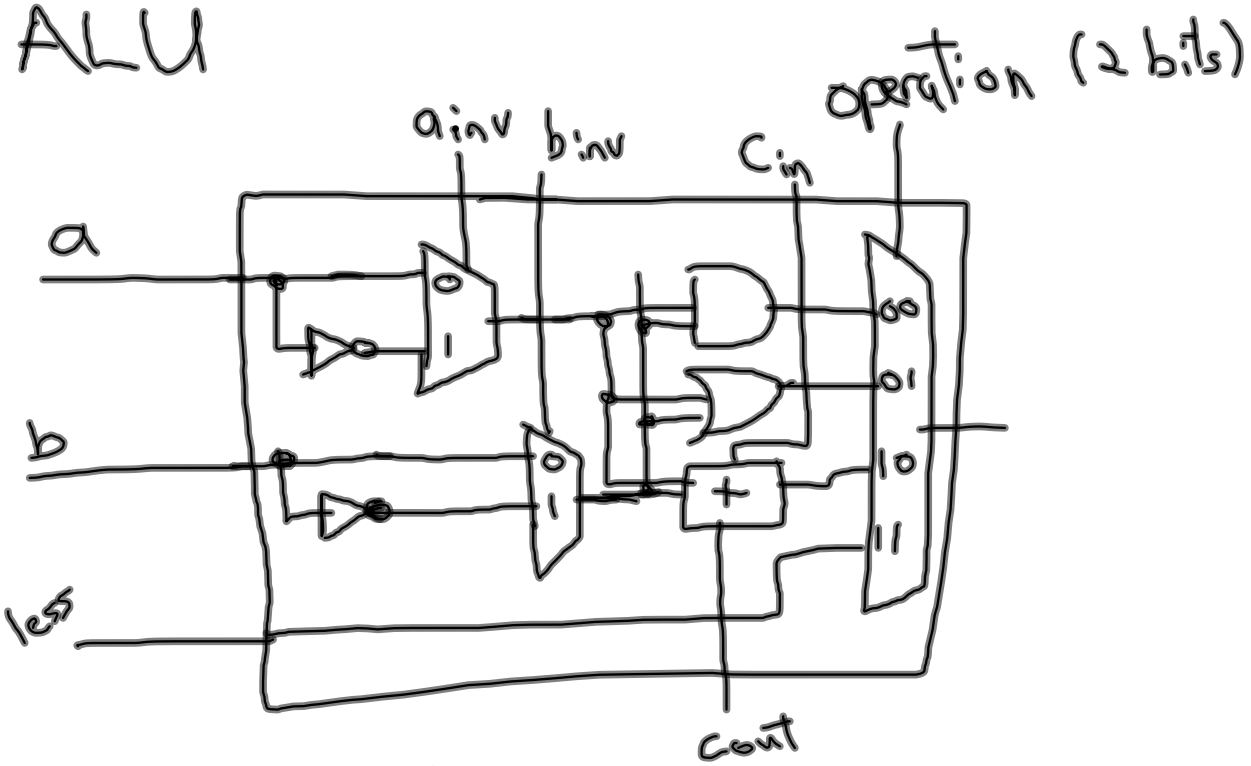

Write
Address
Data
Write data
Data Memory
Read
Bus – multiple wires
32
control

## Registers and ALU




From figures 4.7, 4.8 pp 310-311.

# ALU




| | $a_{inv}$ | $b_{inv}$ | $c_{in}$ | op |
|---|---|---|---|---|
| a+b | 0 | 0 | 0 | 10 |
| a-b | 0 | 1 | 1 | 10 |
| a nor b | 1 | 1 | ⊗ | 00 |

$$\overline{(a \mid b)} = \bar{a} \,\&\, \bar{b}$$

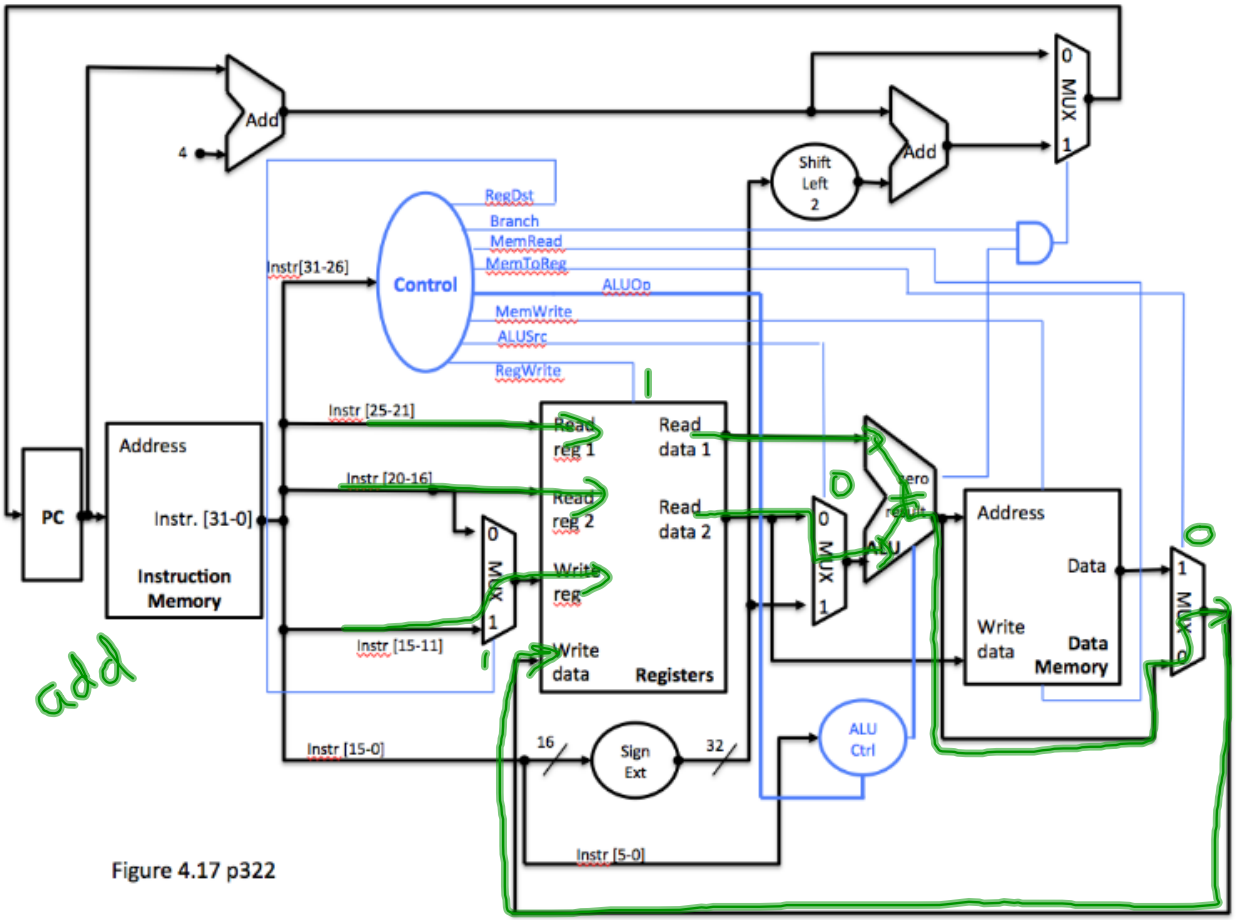



Figure 4.17 p322