Virtual Memory

logical addr → map → physical addr

Stack
↓
heap
↓
data
↓
code

no physical addr. until needed

data

Code
Demand Paging

CPU

Main Mem

Backing Store

page fault

p0-0
p1-0
p1-2
p0-1
p0-3
p2-0
p0-2
p1-1
Page Replacement

F.I.F.O.

ref: 1 1 1 2 7 1 9 2 1 3

next? 4 7 1
Review: no Ch 9

Semaphore
  wait
  signal

Monitors
  Java synchronize
  lock an object
  critical section - all synch methods

Hardware
  Test and set
  compare and swap

atomic
  CPU instructions
Deadlock - safe states

safe

? deadlock

unsafe
CPU Bursts

CPU

running

I/O

wait

CPU

ready

→